UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,347	11/08/2003	Catherine B. Labelle	0180151	4624

25700 7590 06/07/2006

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
CHEN, KIN CHAN	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/705,347
Filing Date: November 08, 2003
Appellant(s): LABELLE ET AL.

Michael Farjami
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed May 1, 2006 appealing from the Office action mailed December 7, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2005/0079696	COLOMBO	4-2005
6,265,260	ALERS et al.	7-2001
6,566,250	TU et al.	5-2003
5,891,798	DOYLE et al.	4-1999
2005/0019964	CHANG et al.	1-2005
6,090,210	BALLANCE et al.	7-2000

6,759,337	ARONOWITZ et al.	7-2004
2005/0019964	CHANG et al.	1-2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 6-8, 14-16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo (US 2005/0079696) in view of Alers et al. (US 6,265,260) or Tu et al. (US 6,566,250) as evidenced by Chang et al. (2004/0188240; [0040]) or Ballance et al. (US 6,090,210; col. 1, lines 32-35), or Aronowitz et al. (US 6,759,337; col. 2, lines 45-50) or Chang et al. (US 2005/0019964; [0041]).

In a method for forming a MOS FET on a substrate, Colombo teaches that a high-k dielectric layer may be situated over the substrate. A gate electrode layer (such as polysilicon) may be thereon. The gate electrode layer and high-k dielectric layer may be etched to form a gate stack. A nitridation process may be performed on the gate stack. Colombo teaches various high-k dielectric materials, reading on instant claims. See abstract; Fig.4; [0010] [0012] [0025] [0029].

Colombo teaches nitridation may be accomplished by any suitable techniques [0011]. Hence, it would have been obvious to one with ordinary skilled in the art to use the conventional nitridation method of applying plasma comprising nitrogen. Alers et al. (US 6,265,260; col. 3, lines 41-43) or Tu et al. (US 6,566,250; col.6, lines 7-9) is only relied on to show the conventional nitridation method of applying plasma comprising nitrogen. Because it is a conventional method in the art of semiconductor device fabrication and because it is disclosed by Alers, Tu, hence, it would have been obvious

to one with ordinary skilled in the art to apply said nitridation method in the process of Colombo in order to efficiently carry out the nitridation process.

As to claim 16, the prior art teaches the limitation because the same nitridation is performed on the gate stack, it is expected that the method of the prior art would contain the same properties and effects (nitrogen forming an oxygen diffusion barrier in the high-k dielectric segment).

Claims differ from prior art by specifying performing the nitridation and etching in the same process chamber. However, It is common in the art that the plasma process chamber may be used for performing both etching and nitridation because it is efficient and more cost effective. See Chang et al. (2004/0188240; [0040]) or Ballance et al. (US 6,090,210; col. 1, lines 32-35), or Aronowitz et al. (US 6,759,337; col. 2, lines 45-50) or Chang et al. (US 2005/0019964; [0041]).

Claims 1, 6-8, 14-16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle et al. (US 5,891,798) in view of Alers et al. (US 6,265,260) or Tu et al. (US 6,566,250) as evidenced by Chang et al. (2004/0188240; [0040]) or Ballance et al. (US 6,090,210; col. 1, lines 32-35), or Aronowitz et al. (US 6,759,337; col. 2, lines 45-50) or Chang et al. (US 2005/0019964; [0041]).

In a method for forming a MOS FET on a substrate, Doyle teaches that a high-k dielectric layer may be situated over the substrate. A gate electrode layer (such as polysilicon) may be thereon. The gate electrode layer and high-k dielectric layer may be etched to form a gate stack. A nitridation process may be performed on the gate stack. See abstract; col. 4 and col. 5.

Doyle teaches nitridation may be accomplished by any suitable techniques [0011]. Hence, it would have been obvious to one with ordinary skilled in the art to use the conventional nitridation method of applying plasma comprising nitrogen. Alers et al. (US 6,265,260; col. 3, lines 41-43) or Tu et al. (US 6,566,250; col.6, lines 7-9) is only relied on to show the conventional nitridation method of applying plasma comprising nitrogen. Because it is a conventional method in the art of semiconductor device fabrication and because it is disclosed by Alers, Tu, hence, it would have been obvious to one with ordinary skilled in the art to apply said nitridation method in the process of Doyle in order to efficiently carry out the nitridation process.

As to claims 6 and 19, Doyle (col. 4, line 2) teaches that any such high dielectric constant material can be used, making the claimed limitation obvious because the claimed high dielectric constant materials are commonly used in the art of semiconductor device fabrication.

As to claim 16, the prior art teaches the limitation because the same nitridation is performed on the gate stack, it is expected that the method of the prior art would contain the same properties and effects (nitrogen forming an oxygen diffusion barrier in the high-k dielectric segment).

Claims differ from prior art by specifying performing the nitridation and etching in the same process chamber. However, It is common in the art that the plasma process chamber may be used for performing both etching and nitridation because it is efficient and more cost effective. See Chang et al. (2004/0188240; [0040]) or Ballance et al. (US

6,090,210; col. 1, lines 32-35), or Aronowitz et al. (US 6,759,337; col. 2, lines 45-50) or Chang et al. (US 2005/0019964; [0041]).

(10) Response to Argument

Appellant has argued that Alers or Tu does not suggest application of its disclosure to plasma nitridation of gate stacks in transistors after the gate etch. It is not persuasive. As has been stated in the office action, Alers or Tu is only relied on to show the conventional nitridation method of applying plasma comprising nitrogen, and the combination of the prior art teaches the limitations.

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. In re Merck &Co., Inc., 800F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellant has argued that Chang'240 or Balance or Aronowitz or Chang'964 does not suggest application of its disclosure to plasma nitridation of gate stacks in transistors after the gate etch. It is not persuasive. As stated in the office action, it is common in the art that the plasma process chamber may be used for performing both etching and nitridation because it is efficient and more cost effective. Chang'240 or Balance or Aronowitz or Chang'964 is simple the evidence to show that "performing both etching and nitridation in the same plasma process chamber" is the common knowledge well known in the art of semiconductor device fabrication.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

K. C Chen

Kin-Chan Chen
Primary Examiner
Art Unit 1765

June 2, 2006

Conferees:

Gregory Mills

Glenn Caldarola